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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 09/976,523
Filed: October 12, 2001
Inventor(s):
Michael C. Dorsey

Examiner: Trimmings, J.
Group/Art Unit: 2133
Atty. Dkt. No: 5681-56300

Title: UTILIZING SLOW ASIC
LOGIC BIST TO
PRESERVE TIMING
INTEGRITY ACROSS
TIMING DOMAINS

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date indicated below.

Erin A. Heter
Printed Name
Signature
August 11, 2004
Date

AMENDMENT; RESPONSE TO OFFICE ACTION OF
May 12, 2004

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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AUG 19 2004

Technology Center 2100

Dear Sir:

This paper is submitted in response to the Office Action of May 12, 2004, to further highlight why the application is in condition for allowance.

Please amend the case as listed below.

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